RIGOL
USB3.0
Test Solution

Application Notes

ANW01100-1220-0002

1 Introduction

USB 3.0 is a USB specification initiated by companies such as Intel. Now, USB 3.0 has been updated to USB 3.2 Gen 1 by USB IF. Nowadays, USB 2.0 has been widely recognized by PC manufacturers, and it's necessary for hardware manufacturers. The maximum transmission bandwidth of USB 2.0 is 480 Mbps (60 MB/s), while that of USB 3.0 is up to 5.0 Gbps (500 MB/s).

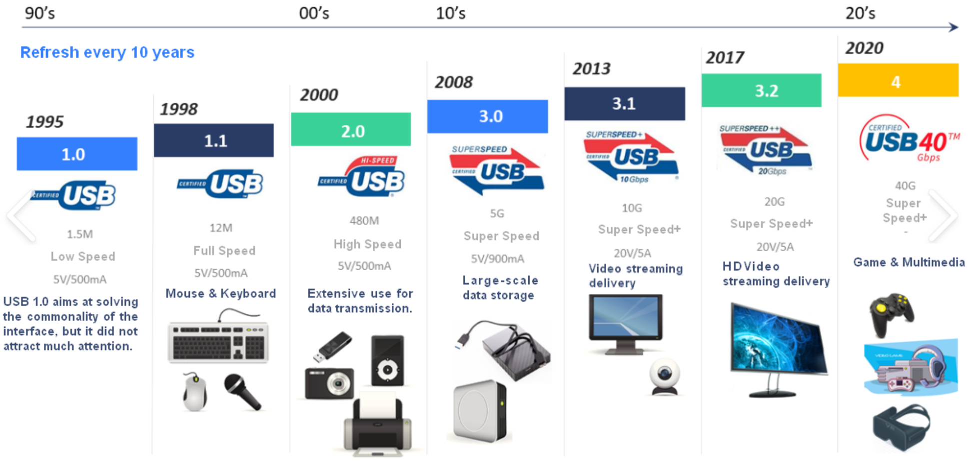


Figure 1.1 USB History

2 USB 3.0

USB 3.0, also known as SuperSpeed USB, has been the standard connector to connect devices to PC or audio/high frequency devices. USB 3.0-related features are only available when USB 3.0-related hardware devices are installed on the computer. Devices from keyboards to high-throughput disk drivers can run smoothly with this low-cost interface for plug-and-play connection with minimal user efforts. The new USB 3.0 offers several enhancements while maintaining compatibility with USB 2.0:

- 5 Gbps full duplex in bandwidth (480 Mbps half duplex for USB 2.0).
- Better power management.
- More power provided from the host to devices with USB such as rechargeable batteries, LED lights and mini fans.
- Faster identification of devices.
- Higher efficiency in data processing.

USB 3.0 can transfer large-volume files such as HD movies at the storage rate defined by the memory device. For example, a USB 3.0 flash drive can transfer 1 GB data to a host in 15 seconds, while USB 2.0 flash drive takes 43 seconds.

Driven by the increasing demand for resolution and memory performance in consumer electronic devices, users need faster transfer performance for broader media applications over broadband Internet connection to make download, storage, and sharing of a large volume of multimedia data faster. USB 3.0 plays a critical role in providing consumers with easy connectivity.

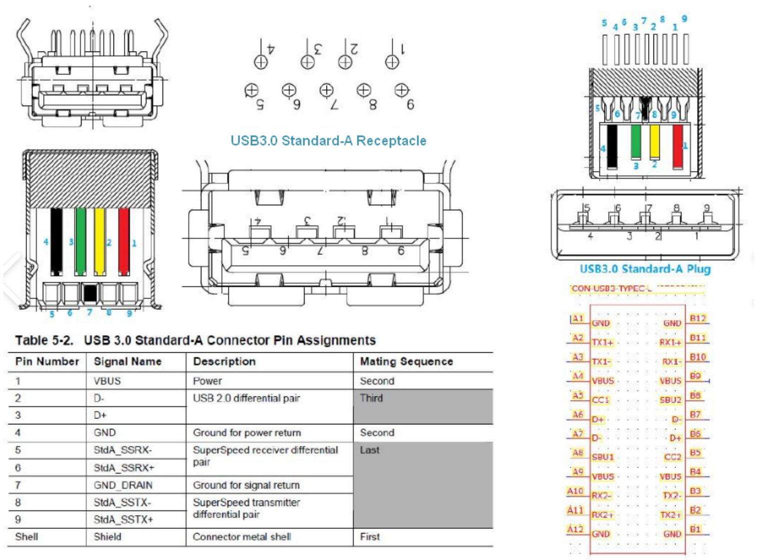


Table 5-2. USB 3.0 Standard-A Connector Pin Assignments

Pin Number	Signal Name	Description	Mating Sequence
1	VBUS	Power	Second
2	D-	USB 2.0 differential pair	Third
3	D+		
4	GND	Ground for power return	Second
5	StdA_SSRX-	SuperSpeed receiver differential pair	Last
6	StdA_SSRX+		
7	GND_DRAIN	Ground for signal return	
8	StdA_SSTX-	SuperSpeed transmitter differential pair	
9	StdA_SSTX+		
Shell	Shield	Connector metal shell	First

Figure 2.1 Definition of USB 3.0 Standard-A Connector Pin

3 Test Challenges

The following table lists the challenges imposed on the test:

Challenges	Analysis
High-speed data transmission requirements	The standard transmission rate of USB 3.0 is 5 Gbps, which requires to use the digital oscilloscope with 13 GHz bandwidth for the test to ensure the stability and reliability of data transmission.
Power management	USB 3.0 needs stable and interference-free power support, which imposes a challenge on the power management test.
Compatibility	USB 3.0 devices need to be tested for compatibility with devices from different manufacturers to ensure stability in different environments.
Signal integrity	The high-speed transmission rate of USB 3.0 imposes high requirements on the signal integrity, and thus a strict signal integrity test is required.
Data analysis	Test results need to be accurately recorded and analyzed to ensure the reliability and accuracy of the test data.

4 Solutions

Devices required in the USB 3.0 test mainly include:

- DS80000 digital oscilloscope
- DG70000 (used for providing trigger signals for the test)
- PC software Rigol CTS
- Text fixture: USB 3.1 DEVICE FIXTURE 1C
- Text fixture: USB 3.1 COMPLIANCE LOAD BOARD
- DP2000 (used for providing power for the test fixture)
- Testing cables

Figure 4.1 DS80000 Used for RIGOL USB 3.0 Test Solution

Figure 4.2 DG70000 Used for RIGOL USB 3.0 Test Solution

Figure 4.3 USB 3.1 Device Fixture 1C Used for RIGOL USB 3.0 Test Solution

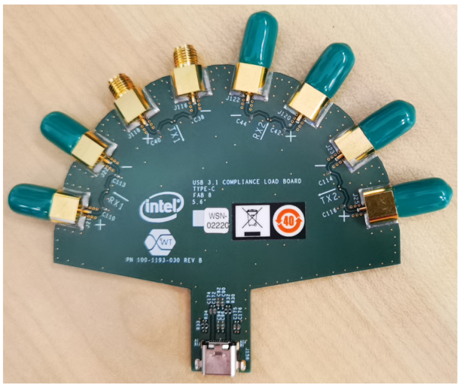


Figure 4.4 USB 3.1 Compliance Load Board Used for RIGOL USB 3.0 Test Solution

The test connection diagram is as follows: First connect two test fixtures Device FIXTURE 1C (Left in figure 4.5) and COMPLIANCE LOAD BOARD (Right in figure 4.5) together by the cable. Connect the DUT to the test port of the Device FIXTURE 1C. Provide a stable power supply of 5V/0.35A for the test fixture Device FIXTURE 1C. Connect the DC+ and DC- of CH1 of the DG70000 to ±TX1 on the COMPLIANCE LOAD BOARD by the cable. Finally, the ± TX1 on the Device FIXTURE 1C is connected to CH1 and CH2 of the oscilloscope DS81304 by the cable.

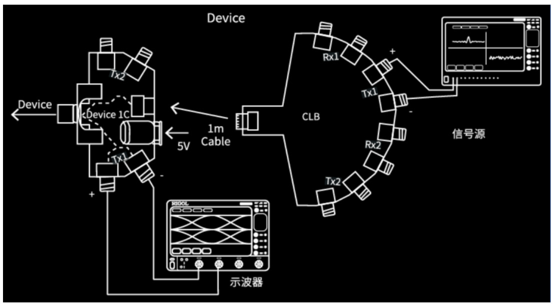


Figure 4.5 Connection Diagram 1 Used for USB 3.0 Test

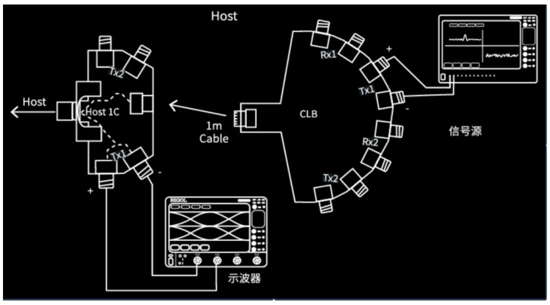


Figure 4.6 Connection Diagram 2 Used for USB 3.0 Test

Figure 4.7 Actual Connection of the Device and the Host

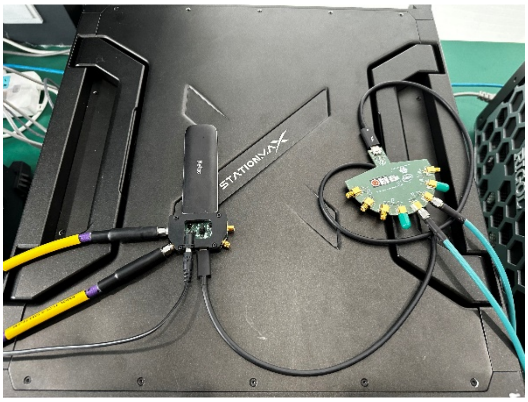


Figure 4.8 Actual Connection of the Fixture and the Device

4.1 Test Solution Features

Features of the RIGOL USB 3.0 compliance test solution are as follows:

1. High-Speed and Stable Acquisition Equipment

DS80000 series digital oscilloscope, the 8th generation of RIGOL's self-developed oscilloscope, is used as the acquisition equipment in the test solution. Based on the StationMAX II platform, DS80000 oscilloscope achieves up to 40 GSa/s real-time sample rate and 13 GHz analog bandwidth. In addition to the improvement in hardware specification, DS80000 series also provides diverse user-friendly designs to ensure the USB 3.0 testing speed required by the customer and the test efficiency.

Figure 4.9 USB 3.0 Test

2. Stable and Pure Power System

DP2000 programmable linear DC power supply is used in the test to provide a high purity voltage signal with low ripple and noise for the test fixture, which eliminates measurement errors caused by power interference. Besides, DP2000 has multiple protection functions, which can effectively prevent the physical damage to expensive test circuits caused by false triggering, misoperation, etc.

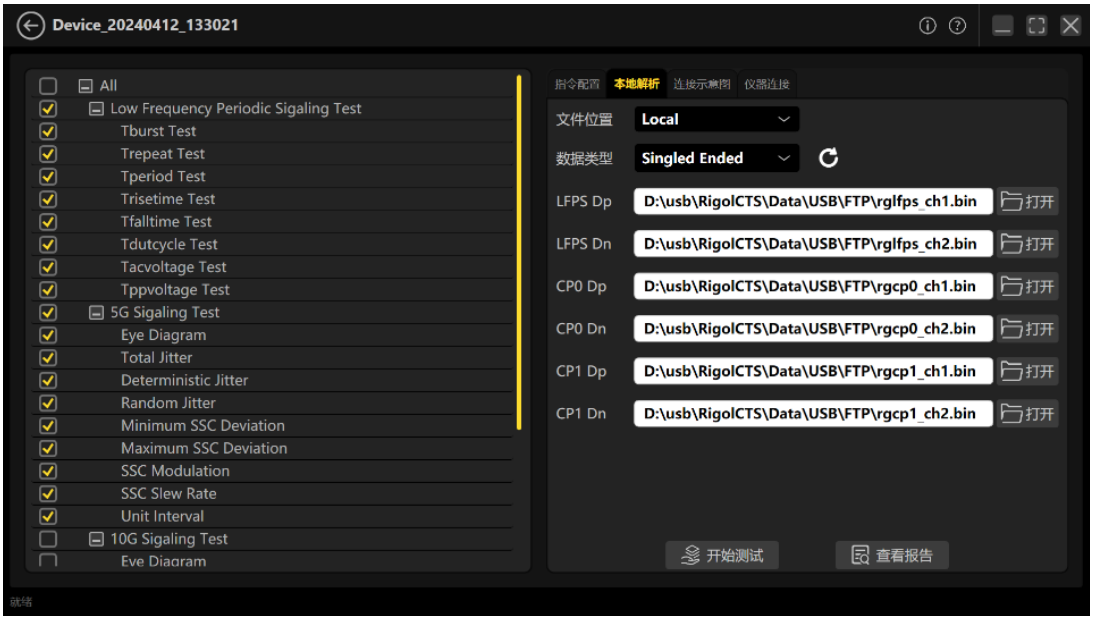
Figure 4.10 DP2000 Provides uA-level Precision Current

3. USB 3.0 Automation Test Analysis Software

RIGOL developed PC automation test software for USB 3.0 test, which can efficiently perform physical layer compliance test. PC software can both be connected to the oscilloscope for automatic test and allows engineers to save data locally for off-line analysis and generates a complete test report.

LFPS signaling test includes pulse burst time, burst repetition interval, clock cycle, pulse rise time, pulse fall time, duty cycle, AC common mode voltage, and differential peak-to-peak value.

5G signaling test includes eye diagram, total jitter, deterministic jitter, random jitter, minimum SSC deviation, maximum SSC deviation, SSC modulation, SSC slew rate, and unit interval.



- ☐ All
  - ☑ Low Frequency Periodic Sigaling Test
    - ☑ Tburst Test
    - ☑ Trepeat Test
    - ☑ Tperiod Test
    - ☑ Trisetime Test
    - ☑ Tfalltime Test
    - ☑ Tdutcycle Test
    - ☑ Tacvoltage Test
    - ☑ Tppvoltage Test
  - ☑ 5G Sigaling Test
    - ☑ Eye Diagram
    - ☑ Total Jitter
    - ☑ Deterministic Jitter
    - ☑ Random Jitter
    - ☑ Minimum SSC Deviation
    - ☑ Maximum SSC Deviation
    - ☑ SSC Modulation
    - ☑ SSC Slew Rate
    - ☑ Unit Interval
  - ☐ 10G Sigaling Test
    - ☐ Eye Diagram

文件位置 Local
数据类型 Singled Ended
LFPS Dp D:\usb\RigolCTS\Data\USB\FTP\rglfps_ch1.bin
LFPS Dn D:\usb\RigolCTS\Data\USB\FTP\rglfps_ch2.bin
CP0 Dp D:\usb\RigolCTS\Data\USB\FTP\rgcp0_ch1.bin
CP0 Dn D:\usb\RigolCTS\Data\USB\FTP\rgcp0_ch2.bin
CP1 Dp D:\usb\RigolCTS\Data\USB\FTP\rgcp1_ch1.bin
CP1 Dn D:\usb\RigolCTS\Data\USB\FTP\rgcp1_ch2.bin

Figure 4.11 USB 3.0 Software Interface

LFPS signal, CP0 signal and CP1 signal should be tested separately in the test as instructed by the PC software and those test signals should be saved on the oscilloscope. Remember that you need to switch the test mode and continue the test after completing saving the specified signal to the oscilloscope. Enter the analysis mode after all signals are tested and saved.

4.2 Test Report

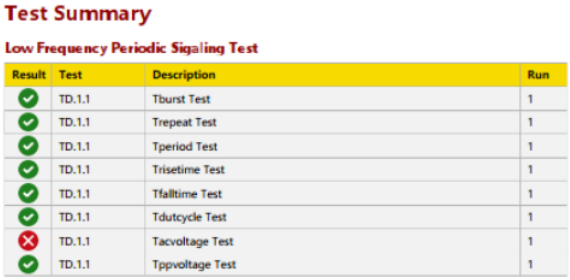
Enter the local analysis mode on PC software after completing all signal tests, and the USB 3.0 PC software will automatically read the waveforms saved by oscilloscope. The SigTest.exe will be recalled, and the analyzed file will generate the USB test item data and output the full USB 3.0 test report.

General Information

DUT Type	Device
Date Time	2023-10-19 19:58:57
Instrument	DS81304
Oscilloscope Version	DS81004
RigolCTS Version	V1.0
Comments	测试USB设备一致性

Figure 4.12 Header of USB 3.0 Compliance Test Report

The first part of the report outlines the general information such as the test time and DUT. Engineers can make adjustments to parameters based on the actual situation.

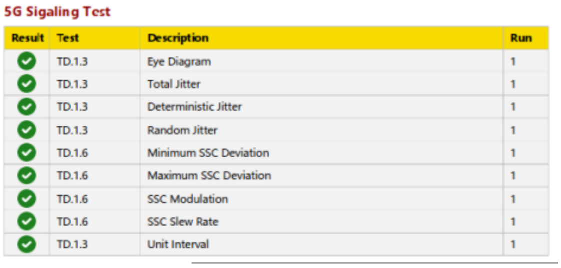


Test Summary

Low Frequency Periodic Sigaling Test

Result	Test	Description	Run
✓	TD.1.1	Tburst Test	1
✓	TD.1.1	Trepeat Test	1
✓	TD.1.1	Tperiod Test	1
✓	TD.1.1	Trisetime Test	1
✓	TD.1.1	Tfalltime Test	1
✓	TD.1.1	Tdutcycle Test	1
✗	TD.1.1	Tacvoltage Test	1
✓	TD.1.1	Tppvoltage Test	1

Figure 4.13 LFPS Signal Test Item of USB 3.0 Compliance Test

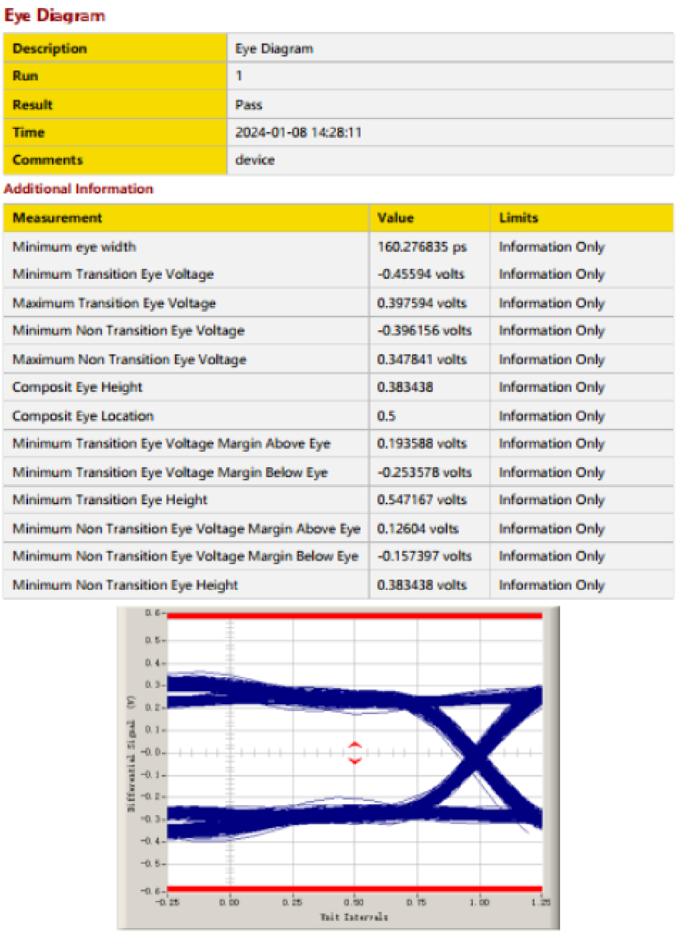


5G Sigaling Test

Result	Test	Description	Run
✓	TD.1.3	Eye Diagram	1
✓	TD.1.3	Total Jitter	1
✓	TD.1.3	Deterministic Jitter	1
✓	TD.1.3	Random Jitter	1
✓	TD.1.6	Minimum SSC Deviation	1
✓	TD.1.6	Maximum SSC Deviation	1
✓	TD.1.6	SSC Modulation	1
✓	TD.1.6	SSC Slew Rate	1
✓	TD.1.3	Unit Interval	1

Figure 4.14 5G Signal Test Item of USB 3.0 Compliance Test

The second part of the report outlines the test summary of all test items. Here, engineers can verify the status of the test item and better judge the test results.

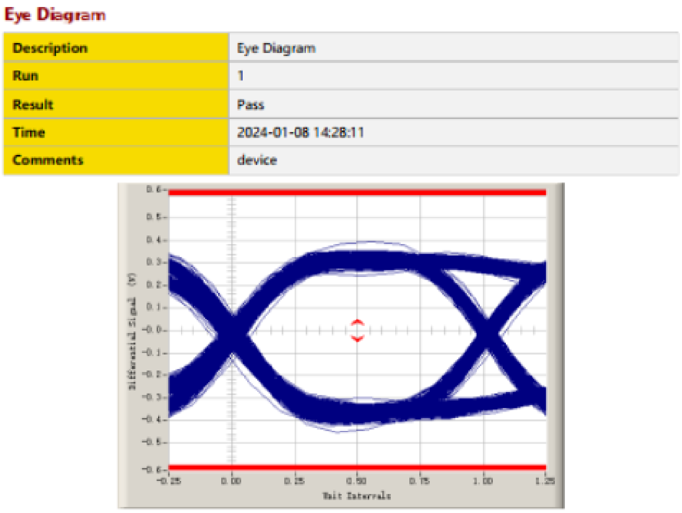


Eye Diagram

Description	Eye Diagram
Run	1
Result	Pass
Time	2024-01-08 14:28:11
Comments	device

Additional Information

Measurement	**Value**	**Limits**
Minimum eye width	160.276835 ps	Information Only
Minimum Transition Eye Voltage	-0.45594 volts	Information Only
Maximum Transition Eye Voltage	0.397594 volts	Information Only
Minimum Non Transition Eye Voltage	-0.396156 volts	Information Only
Maximum Non Transition Eye Voltage	0.347841 volts	Information Only
Composit Eye Height	0.383438	Information Only
Composit Eye Location	0.5	Information Only
Minimum Transition Eye Voltage Margin Above Eye	0.193588 volts	Information Only
Minimum Transition Eye Voltage Margin Below Eye	-0.253578 volts	Information Only
Minimum Transition Eye Height	0.547167 volts	Information Only
Minimum Non Transition Eye Voltage Margin Above Eye	0.12604 volts	Information Only
Minimum Non Transition Eye Voltage Margin Below Eye	-0.157397 volts	Information Only
Minimum Non Transition Eye Height	0.383438 volts	Information Only



Eye Diagram

Description	Eye Diagram
Run	1
Result	Pass
Time	2024-01-08 14:28:11
Comments	device

Figure 4.15 USB 3.0 Compliance Test Report

The third part of the report outlines specific test results of each test item for USB 3.0, including pulse burst time, burst repetition interval, clock cycle and eye diagram, where engineers can observe the specific results of each test item easily. With USB 3.0 compliance test report, engineers can determine whether the DUT is compliant with the USB 3.0 standard.

5 Summary

USB 3.0 interface has higher transmission rate and supports the hot plugging as well as multiple device connections, which meets user needs for ease of use and has become the ultimate choice for most external device manufacturers. However, the rapid improvement in standards and compatibility bring new design challenges that must be addressed for designers.

RIGOL is committed to providing engineers with constantly enhanced solutions. For details, please refer to www.rigol.com.

RIGOL provides a complete set of tools, including digital oscilloscopes, professional test fixtures, and fully automated compliance testing software, enabling USB 3.0 device designers to capture, test and analyze signals efficiently and accurately.

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- Optical Communication

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- New Energy Automobile
- PV/Inverter
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